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Compositions Of Matter, Semiconductor Devices, And Semiconductor Processing Methods

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TECHNICAL FIELD

The invention pertains to compositions of matter comprising silicon bonded to both nitrogen and inorganic material. The invention further pertains to semiconductor devices incorporating the above-described compositions of matter, and to methods of forming semiconductor devices. In particular aspects, the invention pertains to semiconductor devices incorporating copper-containing materials, and to methods of forming such devices.

BACKGROUND OF THE INVENTION

It would be desirable to employ copper-containing materials in semiconductor devices. Copper has conductive properties that are superior to those of many of the conductive materials presently utilized in semiconductor devices. Unfortunately, copper has a drawback associated with it that it cannot generally be placed against oxide-comprising insulative materials (such as, for example, silicon dioxide). If copper-containing materials are placed adjacent oxide-comprising insulative materials, oxygen can diffuse into the copper-containing material and react to reduce conductivity of the material. Also, copper can diffuse into the oxide-containing material to reduce the insulative properties of the oxide-containing material. Additionally, copper can

diffuse through oxide insulative material to device regions and cause degradation of device (e.g., transistor) performance. The problems associated with copper are occasionally addressed by providing nitride-containing barrier layers adjacent the copper-containing materials, but such can result in problems associated with parasitic capacitance, as illustrated in Fig. 1. Specifically, Fig. 1 illustrates a fragment of a prior art integrated circuit, and illustrates regions where parasitic capacitance can occur.

The structure of Fig. 1 comprises a substrate 10, and transistor gates 12 and 14 overlying substrate 10. Substrate 10 can comprise, for example, monocrystalline silicon lightly doped with a p-type background conductivity-enhancing dopant. To aid in interpretation of the claims that follow, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Transistor gates 12 and 14 can comprise conventional constructions such as overlying layers of gate oxide, polysilicon and silicide. Insulative spacers 16 are formed adjacent transistor gates 12 and 14,

and conductively doped diffusion regions 18, 20 and 22 are formed within substrate 10 and proximate gates 12 and 14. Also, isolation regions 24 (shown as shallow trench isolation regions) are formed within substrate 10 and electrically isolate diffusion regions 18 and 22 from other circuitry (not shown) provided within and over substrate 10.

An insulative material 26 extends over substrate 10, and over transistor gates 12 and 14. A conductive plug 28 extends through insulative material 26 to contact conductive diffusion region 20. Conductive plug 28 can comprise, for example, conductively doped polysilicon. Insulative material 26 can comprise, for example, silicon dioxide or borophosphosilicate glass (BPSG). Insulative material 26 and plug 28 together comprise a planarized upper surface 29. Planarized surface 29 can be formed by, for example, chemical-mechanical polishing.

A second insulative material 30 is formed over insulative material 26 and on planarized upper surface 29. Second insulative material 30 can comprise, for example, borophosphosilicate glass or silicon dioxide. A conductive material 32 is formed within an opening in insulative material 30 and over conductive plug 28. Conductive material 32 comprises copper. The copper can be, for example, in the form of elemental copper, or in the form of an alloy. Conductive material 32 is separated from conductive plug 28 by an intervening barrier layer 34. Barrier layer 34 typically comprises a conductive material, such as titanium nitride (TiN) or tantalum nitride (TaN), and

is provided to prevent out-diffusion of copper from conductive material 32 into either insulative material 26 or the polysilicon of conductive plug 28. Barrier layer 34 can also prevent diffusion of silicon or oxygen from layers 26, 28 and 30 into the copper of conductive material 32. It is desired to prevent diffusion of oxygen to the copper of material 32, as such oxygen could otherwise reduce conductance of material 32. Also, it is desired to prevent copper diffusion from material 32 into insulative layer 26, as such copper could reduce the insulative properties of the material of layer 26. Additionally, diffusion through layer 26 and into one or more of regions 18, 20 and 22 can reduce the performance of transistor devices.

A second conductive material 36 is provided over insulative material 26 and spaced from first conductive material 32. Second conductive material 36 can comprise, for example, conductively doped polysilicon or a conductive metal, or a combination of two or more conductive materials (such as copper and TiN). Second conductive material 36 is spaced from first conductive material 32 by an intervening region of insulative material 30 and barrier layer 34.

Insulative material 30, barrier layer 34, first conductive material 32 and second conductive material 36 share a common planarized upper surface 37. Planarized upper surface 37 can be formed by, for example, chemical-mechanical polishing.

An insulative barrier layer 38 is provided over planarized upper surface 37. Insulative barrier layer 38 can comprise, for example, silicon nitride.

An insulative layer 40 is provided over insulative barrier layer 38. Insulative layer 40 can comprise, for example, silicon dioxide or BPSG. Insulative barrier layer 38 inhibits diffusion of copper from first conductive material 32 into insulative layer 40, and inhibits diffusion of oxygen from insulative layer 40 into first conductive material 32.

Another insulative layer 42 is provided over insulative layer 40, and a third conductive material 44 is provided within insulative material 42 and over first conductive material 32. Insulative material 42 can comprise, for example, BPSG or silicon dioxide, and third conductive material 44 can comprise, for example, conductively doped polysilicon or a metal, or a combination of two or more conductive materials (such as copper and TiN).

Conductive materials 32, 36 and 44 can be conductive interconnects between electrical devices, or portions of electrical devices. The function of materials 32, 36 and 44 within a semiconductor circuit is not germane to this discussion. Instead, it is the orientation of conductive materials 32, 36 and 44 relative to one another that is of interest to the present discussion. Specifically, each of materials 32, 36 and 44 is separated from the other materials by intervening insulative (or dielectric) materials. Accordingly, parasitic capacitance can occur

between the conductive materials 32, 36 and 44. A method of reducing the parasitic capacitance is to utilize insulative materials that have relatively low dielectric constants ("k"). For instance, as silicon dioxide has a lower dielectric constant that silicon nitride, it is generally preferable to utilize silicon dioxide between adjacent conductive components, rather than silicon nitride. However, as discussed previously, copper-containing materials are preferably not provided against silicon dioxide due to diffusion problems that can occur. Accordingly, when copper is utilized as a conductive material in a structure, it must generally be spaced from silicon dioxide-comprising insulative materials to prevent diffusion of oxygen into the copper structure, as well as to prevent diffusion of copper into the oxygen-comprising insulative material. Accordingly, the copper materials are generally surrounded by nitride-comprising materials (such as the shown barrier layers 34 and 38) to prevent diffusion from the copper materials, or into the copper materials. Unfortunately, this creates the disadvantage of having relatively high dielectric constant nitride materials (for example, the material of layer 38) separating conductive materials. Accordingly, the requirement of nitride-comprising barrier layers can take away some of the fundamental advantage of utilizing copper-comprising materials in integrated circuit constructions.

SUMMARY OF THE INVENTION

In one aspect, the invention encompasses a semiconductor processing method wherein a conductive copper-containing material is formed over a semiconductive substrate and a second material is formed proximate the conductive material. A barrier layer is formed between the conductive material and the second material. The barrier layer comprises a compound having silicon chemically bonded to both nitrogen and an organic material.

In another aspect, the invention encompasses a composition of matter comprising silicon chemically bonded to both nitrogen and an organic material.

In yet another aspect, the invention encompasses a semiconductor processing method. A semiconductive substrate is provided and a layer is formed over the semiconductive substrate. The layer comprises a compound having silicon chemically bonded to both nitrogen and an organic material.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic, cross-sectional, fragmentary view of a prior art integrated circuit construction.

Fig. 2 is a diagrammatic, cross-sectional, fragmentary view of an integrated circuit construction encompassed by the present invention.

Fig. 3 is a diagrammatic, cross-sectional, fragmentary view of another embodiment integrated circuit construction encompassed by the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

In accordance with one aspect of the present invention, a novel composition of matter has been developed which comprises silicon chemically bonded to both nitrogen and an organic material, and wherein the nitrogen is not bonded to carbon. More specifically, the silicon is chemically bonded to both nitrogen and carbon. The carbon can be, for example, in the form of a hydrocarbon. In a preferred aspect, the carbon is comprised by a methyl group and the composition of matter consists essentially of $(CH_3)_xSi_3N_{(4-x)}$, wherein x is greater than 0 and no greater than about 4.

A composition of the present invention can be formed by, for example, reacting inorganic silane with one or more of ammonia (NH_3), hydrazine (N_2H_4), or a combination of nitrogen (N_2) and hydrogen (H_2). The reaction can occur with or without a plasma. However, if the

reaction comprises an organic silane in combination with dinitrogen and dihydrogen, the reaction preferably occurs in the presence of plasma.

An exemplary reaction is to combine methylsilane (CH_3SiH_3) with ammonia (NH_3) in the presence of a plasma to form $(CH_3)_xSi_3N_{4-x}$. The exemplary reaction can occur, for example, under the following conditions. A substrate is placed within a reaction chamber of a reactor, and a surface of the substrate is maintained at a temperature of from about 0°C to about 600°C. Ammonia and methylsilane are flowed into the reaction chamber, and a pressure within the chamber is maintained at from about 300 mTorr to about 30 Torr, with a plasm at radio frequency (RF) power of from about 50 watts to about 500 watts. A product comprising $(CH_3)_xSi_3N_{(4-x)}$ is then formed and deposited on the substrate. The reactor can comprise, for example, a cold wall plasma reactor.

It is found that the product deposited from the described reaction consists essentially of Si_3N_y and $(CH_3)_xSi_3N_{(4-x)}$, (wherein y is generally about 4/3, and x is also generally about 4/3). The $(CH_3)_xSi_3N_{(4-x)}$ is present in the product to a concentration of from greater than 0% to about 50% (mole percent), and is preferably from about 10% to about 20%. The amount of $(CH_3)_xSi_3N_{(4-x)}$ present in the product can be adjusted by providing a feed gas of SiH_4 in the reactor in addition to the CH_3SiH_3, and by varying a ratio of the SiH_4 to the CH_3SiH_3, and/or by adjusting RF power.

The compositions of matter encompassed by the present invention are found to be insulative, and to have lower dielectric constants than silicon nitride. Accordingly, compositions of the present invention can be substituted for silicon nitride in barrier layers to reduce parasitic capacitance between adjacent conductive components. Fig. 2 illustrates a fragment of an integrated circuit incorporating a composition of the present invention. In referring to Fig. 2, similar numbering to that utilized above in describing the prior art structure of Fig. 1 will be used, with differences indicated by different numerals.

The structure of Fig. 2 differs from the prior art structure of Fig. 1 in that Fig. 2 illustrates a barrier layer 100 in place of the silicon nitride barrier layer 38 of Fig. 1. Layer 100 can comprise, for example, an above-described novel composition of the present invention, such as, for example, $(CH_3)_xSi_3N_{(4-x)}$. Alternatively, layer 100 can comprise a composition which includes carbon, silicon and nitrogen, and wherein the nitrogen is bonded to carbon. Layer 100 is proximate conductive material 32 (actually against conductive material 32) and separates second conductive material 44 from first conductive material 32. In the construction shown in Fig. 2, barrier layer 100 separates conductive material 32 from an insulative material 40 to impede migration of oxide from insulative material 40 into copper of a preferred conductive material 32, as well as to impede migration of copper from preferred material 32 into insulative material 40.

Fig. 3 illustrates an alternate embodiment semiconductor construction of the present invention (with numbering identical to that utilized in Fig. 2), wherein insulative material 40 (Fig. 2) is eliminated. Barrier layer 100 is thus the only material between first conductive material 32 and second conductive material 44, and is against both conductive material 32 and conductive material 44.

In exemplary embodiments of the present invention, barrier layer 100 comprises $(CH_3)_xSi_3N_{(4-x)}$ (wherein "x" is from about 1 to about 4, and preferably wherein "x" is about 0.7). Such barrier layer 100 can be formed by the methods discussed above, and can, for example, consist essentially of Si_3N_y and $(CH_3)_xSi_3N_{(4-x)}$. Also, an amount of $(CH_3)_xSi_3N_{(4-x)}$ within barrier layer 100 can be adjusted by the above-discussed methods of adjusting a ratio of SiH_4 and CH_3SiH_3 during formation of the layer. An exemplary concentration of $(CH_3)_xSi_3N_{(4-x)}$ within barrier layer 100 is from greater than 0% to about 20% (mole percent).

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or

modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.